REMARKS/ARGUMENTS

1. Claim Amendments

The Applicant has amended claims 1, 12-14, 18, 21, 24, 27, 30, 33 and 36. Furthermore, claims 8, 23, 29 and 35 have been cancelled. Applicant respectfully submits no new matter has been added. Accordingly, claims 1-7, 9-22, 24-28, 30-34 and 36-38 are pending in the application. Favorable reconsideration of the application is respectfully requested in view of the foregoing amendments and the following remarks.

2. Examiner Objections – Specification

In paragraphs 1 and 2 of the Office Action, the Examiner objected to the abstract of the disclosure because it contained legal phraseologies. The Applicants have amended the abstract to overcome the objection.

3. Claim Rejections – 35 U.S.C. § 112

Claims 12-14, 18, 24, 30, and 36 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant has amended claims 12-14, 18, 24, 30 and 36 to overcome the rejection.

4. Claim Rejections – 35 U.S.C. § 102(b)

Claims 1-17 and 19-38 stand rejected under 35 U.S.C. 102(b) as being anticipated by *Purcell et al* (US 5,598,514, hereinafter Purcell). The Applicant has amended claims 1, 21, 27 and 33 to provide that, with respect to the storage of new data in the second format, *wherein the second format comprises chrominance and*

luminance data in an interleaved YCbCr 4:2:0 format. Support for amendments to claims 1, 21, 27, and 33 can be found at least in Figure 9, and paragraph [0039] of the present application. The Examiner states (emphasis added):

> With respect to claims 2-17 and 19-38, Purcell et al also discloses the stored data contains image data from a previous flame (Fig. 17); the block of current video data in the first format is a portion of a current flame (e.g. intra-frame); the stored data in the second format is a portion of a previously coded frame (e.g. inter-frame); the second format comprises reduced chrominance information 204 as compared to the first format; *the first format and the second format comprises interleaved chrominance and luminance data (Fig. 6);* each block of a video frame comprises a predefined grouping of pixels (Fig. 16); encoding the block of the current video frame comprises compressing the block of the current video frame (e.g. MPEG) by comparing the block of the current video frame to a corresponding block of another video frame: comparing the block of the current video frame to a corresponding block of another video frame is preceded by retrieving the corresponding block of the other video frame in the second format 204; transferring the new data in the second format to a memory location 103; and storing the new data for encoding of a corresponding block of a subsequent video frame (Fig. 18); storing the encoded video data in a third format in a buffer (e.g. DRAM); and transferring the buffered data to a memory location 103 on completion of encoding the block; transferring a portion of the block of video data from the buffer to the memory 103 location if the buffer is full prior to encoding the entire block of video data: encoding the block of current video data 111 using the data stored in the second format is preceded by converting a block of a data in the first format to the second format 204; and the block of current video data comprises a micro-block [sic] line of video data (e.g. tiles of MB).

Figures 6(a)-(e) of Purcell disclose:

> FIG. 6a is a block diagram of interpolator 206.
>
> FIG. 6b is an address map of video FIFO 205, showing the partition of video FIFO 205 into Y region 651, U region 652 and V region 653, and the storage locations of data in a data stream 654 received from decimator 204.

FIG. 6c illustrates the generation of addresses for accessing video FIFO 205 from the contents of address counter 207, during YUV separation, or during video output.

FIG. 6d illustrates the sequence in which stored and interpolated luminance and chrominance pixels are output under interpolation mode.

FIG. 6e shows two block interleaved groups 630 and 631 in video FIFO 205.

None of the descriptions of the foregoing Figures disclose the element of *wherein the second format comprises chrominance and luminance data in an interleaved YCbCr 4:2:0 format*. According to Purcell:

FIG. 6a shows interpolator 206 of chip 100. As shown in FIG. 6a, during video output mode, an address generator 601, which includes address counters 207 and 208, is provided to read from video FIFO 205 samples of video data. Consecutive samples of video data of the same type are latched into 8-bit registers 602 and 603. Data contained in register 602 and 603 are provided as input operands to adder 604. Each result of adder 604 is divided by 2, i.e. right-shifted by one bit, and latched into register 605. In this embodiment, registers 602 and 603 are clocked at 60 Mhz, and register 605 is clocked at 30 Mhz.

When video bus 109a is configured as an input bus, video FIFO 205 receives from decimator 204 the decimated video data, which is then transferred to external memory 103. Alternatively, when video bus 109a is configured as an output bus, video data are received from external memory 103 and provided in a proper sequence to interpolator 206 for output to video bus 109a. The operation of the video FIFO in video port 107 is similar to that of video FIFO 205.

When YUV separation is performed during input mode, or when interpolation is performed during output mode, video FIFO 205 is divided into four groups of locations ("block interleaved groups"). Each block interleaved group comprises a 16-byte "Y-region", an 8-byte "U-region", and an 8-byte "V-region". Data transfers between video FIFO 205 and external memory 103 occur as DMA accesses under memory controller 104's control. Address counters 207 and 208 generate the addresses required to access video FIFO 205.

FIG. 6b is an address map 650 of a block interleaved group in video FIFO 205, showing the block interleaved group partitioned into Y-

region 651, U-region 652 and V-region 653. A data stream 654 arriving from decimator 204 is shown at the top of address map 650. Shown in each of the regions are the locations of data from data stream 654.

Address map 650 also represents the data storage location for performing interpolation, when video port 107 is configured as an output port. As shown in FIG. 6b, the Y-region 651 is offset from the U-region 652 by sixteen bytes, and the U-region 652 is further offset from the V-region 653 by eight bytes. In addition, adjacent groups of block interleaved locations are offset by 32 bytes.

Address counter 207 generates the addresses of video FIFO 205 for YUV separation during input mode, and the addresses for interpolation during output mode. FIG. 6c illustrates address generation by address counter 207 for accessing video FIFO 205. As shown in FIG. 6c, address counter 207 comprises a 11-bit counter 620 counting at 60 Mhz. Embedded fields in counter 620 include a 9-bit value C[8:0], and bits "p" and "ex". The positions of these bits in counter 620 are shown in FIG. 6c. The "p" bit, which is the least significant bit of counter 620, represents the two phases of an interpolation operation. These two phases of an interpolation operation correspond to operand loadings into registers 602 and 603 (FIG. 6a) during the (1, 1) interpolation.

During interpolation, every other luminance sample, every other red type chrominance sample (Cr), and every other blue chrominance sample (Cb) are interpolated. FIG. 6d shows, under interpolation mode, the sequence in which stored and interpolated luminance and chrominance samples are output.

Bit C[0] of binary counter 620 counts at 30 MHz. Since video data samples are received or output at video ports 107 and 108 in pixel interleaved order at 30 MHz, bit C[0] of binary counter 620 indicates whether a luminance sample or a chrominance sample is received or output. Since bit C[1] counts at half the rate of bit C[0], for chrominance samples, bit C[1] indicates whether a Cb or a Cr type chrominance sample is output.

Bits C[8:0] are used to construct the byte address B[8:0] (register 625) for accessing video FIFO 205. Bits B[6:5] indicate which of the four block interleaved groups in video FIFO 205 is addressed. Thus, bits B[8:5] form a "group address". Incrementer 621 receives bits C[8:2] and, during interpolation, increments the number represented by these bits. Bits C[8:2] is incremented whenever the following expression evaluates to a logical true value:

where is the logical operator "and" and is the logical operator "or". Bit "ex" of binary counter 620 indicates an interpolation output. Thus, according to this expression, incrementer 621 increments C[8:2] at one of the two phases of the interpolation operation, every other luminance output, or every other blue or red chrominance output. In this embodiment, when the output sample is not an interpolated output sample, incrementer 621 is disabled. Consequently, both registers 602 and 603 (FIG. 6a) obtain their values from the same byte address. In effect, the same sample is fetched twice, so that each non-interpolated sample is really obtained by performing a 1--1 interpolating using two identical values.

The data output of incrementer 621 is referenced as D[6:0]. As shown in FIG. 6c, the group address B[6:5] is provided by bits D[4:3]. Since a toggle of bit B[4] indicates a jump of 16 byte addresses, bit B[4] can be used to switch, within a block interleaved group, between the luminance and the chrominance regions. Accordingly, bit B[4] adopts the value of negated bit C[0]. In addition, since a toggle of bit B[3] indicates a jump of eight byte addresses, bit B[3] can be used to switch, when a chrominance sample is fetched, between the U and V regions of a block interleaved group. Thus, as shown in FIG. 6c, bit B[3] has the value of bit C[1].

The unregistered value 624 contains a value E[4:0] formed by the ordered combination of bit C[1], bits D[2:0] and the bit which value is provided by the expression ((C[1]p)ex), where is the "exclusive-or" operator. Bits E[4:l] provides the byte address bits B[3:0] during output of a chrominance sample, and bits E[3:0] provides byte address bits B[3:0] during output of a luminance sample. Bit E[0] ensures the correct byte address is output when an "odd" interpolated luminance sample is output. (U+V refer to chrominance pixel types Cb +Cr respectively.)

FIG. 6e shows two adjacent block interleaved groups 630 and 631. Group 630 comprises Y-region 630a, U-region 630b and V-region 630c and group 631 comprises Y-region 631a, U-region 631b and V-region 631c. In FIG. 6e, the labels 1-31 in group 630 represent the positions, in pixel interleaved order, of the pixels stored at the indicated locations of video FIFO 205. Likewise, the labels 32-63 in group 631 represent the positions, in pixel interleaved order, of the pixels stored at the indicated locations. The control structure of FIG. 6c ensures that the proper group addresses are generated when the output sequence crosses over from output samples obtained or interpolated from pixels in group 630 to samples obtained or interpolated from pixels in group 631.

In the present invention, Figure 9, and its accompanying description in paragraph [0039] provide as follows:

> A video encoder converts the macro block of data from the input buffer to a second format. In some embodiments, a separate video encoder may be provided to convert the macro block of data from the input buffer to the second format. The second format can be an interleaved YCbCr 4:2:0 format, such as the interleaved YCbCr 4:2:0 format shown in Fig 9. An interleaved format may facilitate the processing of video data in blocks because the chrominance and luminance data is interleaved within a memory, rather than being stored in separate memory blocks, such as in non-interleaved YCbCr 4:2:0 format as shown in Fig 8. Accordingly, fewer memory read operations may be needed to transfer the interleaved data between the memory and the processor than may be required when the chrominance and luminance data is not interleaved...

5. Claim Rejections – 35 U.S.C. § 103 (a)

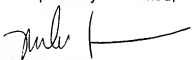
Claim 18 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Purcell. As noted above, Applicant has amended claim 1, from which claim 18 depends, to better define the intended scope of the claimed invention. The Examiner's consideration of the amended claim is respectfully requested.

CONCLUSION

In view of the foregoing remarks, the Applicant believes all of the claims currently pending in the Application to be in a condition for allowance. The Applicant. therefore, respectfully requests that the Examiner withdraw all rejections and issue a Notice of Allowance for all pending claims.

The Applicant requests a telephonic interview if the Examiner has any questions or requires any additional information that would further or expedite the prosecution of the Application.

Respectfully submitted,



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